Design, test and reliability aspects of analog compute-in-memory AI accelerators: my group's recent experience

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Résumé

Compute In Memory (CIM) is becoming a computing architecture of reference to build energy-efficient processors dedicated to AI tasks, known as AI accelerators. Although we can build CIM computing core digitally, achieving further 10-100x improvements in energy efficiency, necessary for the next generation of embedded AI systems, may rely on analog computing principles. Specifically, emerging Non-Volatile Memories (eNVMs) offer a promising path toward storing and computing AI data more efficiently. Yet, building complete AI systems integrating reliable analog CIM computing cores is not straightforward. At least, that is what my group has experienced in the past 4 to 5 years. Examples of these challenges are: (1) integrating CIM cores into complete systems, for instance, with a digital control processor, (2) how to limit the variability of analog circuitries to ensure sufficient computation, or (3) how to automatically program and test AI accelerator systems. Hence, in this talk, I will walk you through how my group approaches the design of analog CIM circuits, focusing on these practical aspects that are typically not fully explained. Examples of challenges we face(d) are designing an effective analog computing cell, designing circuit peripherals, integrating the CIM core into a full system, and ensuring more reliability and accuracy in the system through self-calibration.